590 C-V Analyzer

590/100k and 590/100k/M Front Panel Specifications

100 kHz (4½ Digits)

RANGE	RESOLUTION	ACCURACY (1 Year)[2] 18°–28°C ±(%rdg + counts)	P-P NOISE[5] FILTER ON	TEMPERATURE COEFFICIENT 0°–18°C & 28°–50°C ±(%rdg + counts)/°C	SHUNT CAPACITANCE LOADING EFFECT[4] ±(%rdg + counts)
2 pF	0.1 f F	0.12% + (500 × G/G_{FS} + 200)	6 f F	0.02% + (20 × G/G_{FS})	0.1 % + (3 × G/G_{FS})
2 µS	0.1 nS	0.12% + (50 × C/C_{FS} + 200)	4 nS	0.02% + (7 × C/C_{FS})	0.1 % + (3 × C/C_{FS})
20 pF	1 f F	0.12% + (260 × G/G_{FS} + 10)	6 f F	0.02% + (20 × G/G_{FS})	0.1 % + (3 × G/G_{FS})
20 µS	1 nS	0.12% + (22 × C/C_{FS} + 10)	4 nS	0.02% + (7 × C/C_{FS})	0.1 % + (3 × C/C_{FS})
200 pF	10 f F	0.12% + (260 × G/G_{FS} + 5)	90 f F	0.02% + (20 × G/G_{FS})	0.1 % + (3 × G/G_{FS})
200 µS	10 nS	0.12% + (22 × C/C_{FS} + 5)	60 nS	0.02% + (7 × C/C_{FS})	0.1 % + (7 × C/C_{FS})
2 nF	100 f F	0.12% + (260 × G/G_{FS} + 5)	900 f F	0.02% + (20 × G/G_{FS})	0.02% + (2 × G/G_{FS})
2 mS	100 nS	0.12% + (22 × C/C_{FS} + 5)	0.6 µS	0.02% + (7 × C/C_{FS})	0.02% + (3 × C/C_{FS})
20 nF *	1 pF	0.25% + (260 × G/G_{FS} + 5)[3]	9 pF	0.1 % + (30 × G/G_{FS})	0.02% + (2 × G/G_{FS})
20 mS	1 µS	0.25% + (22 × C/C_{FS} + 5)	6 µS	0.1 % + (10 × C/C_{FS})	0.02% + (2 × C/C_{FS})

Accuracy is maximum limit for Q≥20; typical for Q<20.

*Using Model 5904 20nF/20mS Input Adapter.

590/1M and 590/100k/M Front Panel Specifications

1 MHz (4½ Digits)

RANGE	RESOLUTION	ACCURACY (1 Year)[2] 18°–28°C ±(%rdg + counts)	P-P NOISE[5] FILTER ON	TEMPERATURE COEFFICIENT 0°–18°C & 28°–50°C ±(%rdg + counts)/°C	SHUNT CAPACITANCE LOADING EFFECT[4] ±(%rdg + counts)
20 pF	1 f F	0.29% + (300 × G/G_{FS} + 10)	6 f F	0.02% + (20 × G/G_{FS})	0.5 % + (25 × G/G_{FS})
200 µS	10 nS	0.29% + (120 × C/C_{FS} + 10)	40 nS	0.02% + (8 × C/C_{FS})	0.5 % + (10 × C/C_{FS})
200 pF	10 f F	0.29% + (300 × G/G_{FS} + 5)	100 f F	0.02% + (20 × G/G_{FS})	0.35% + (40 × G/G_{FS})
2 mS	100 nS	0.29% + (120 × C/C_{FS} + 5)	700 nS	0.02% + (8 × C/C_{FS})	0.35% + (16 × C/C_{FS})
2 nF	100 f F	0.29% + (300 × G/G_{FS} + 5)	200 f F	0.02% + (20 × G/G_{FS})	0.35% + (40 × G/G_{FS})
20 mS	1 µS	0.29% + (120 × C/C_{FS} + 5)	1 µS	0.02% + (8 × C/C_{FS})	0.35% + (16 × C/C_{FS})

Accuracy is maximum limit for Q≥20; typical for Q<20.

NOTES:

1. G = conductance reading; C = capacitance reading; G_{FS} = full scale conductance; C_{FS} = full scale capacitance. Range and accuracy designations based on parallel RC model.
2. Front panel accuracy is relative to calibration source accuracy. Add front panel accuracy and source accuracy for total accuracy. Factory calibration source accuracy is 0.06% for 100kHz and 0.08% for 1MHz. CAL is used to cancel initial zero, gain, and phase error terms within 8 hours of measurement or whenever ambient temperature changes by more than 2°C.
3. The 5904 must be calibrated with a particular 590/100k to achieve specified accuracy.
4. "Shunt Capacitance Loading" is additional accuracy with equal shunt load on Output and Input, per 100pF shunt load.
5. Noise specified with 500pF shunt loading on Output and Input. Noise on 2pF and 20pF ranges is typical with 100pF shunt load; 500pF will increase noise no more than ×2. Measured at 10 rdg/s rate.

CAPACITANCE NON-LINEARITY: <0.1% of range, for Q > 20 or D < 0.05, 18°–28°C.

TEST VOLTAGE: 15mV rms ±10%.

TEST FREQUENCY: 590/100k: 100kHz. 590/1M: 1MHz. Tolerance: ±0.1%.

ANALYSIS CAPABILITY

(Programming & output available from front panel or IEEE-488 bus)

READING BUFFERS A and B: Two data buffers allow storage and mathematical manipulation on up to 450 measurement triplets: capacitance, conductance, and voltage. In C vs. t, capacitance and index only are stored (up to 1350 points).

$1/C^2$: Performs the inverse of C^2 on the capacitance data stored in reading buffer.

C/C_O: Allows normalization of capacitance readings stored in reading buffer to a user-programmable reference value C_O.

C_{MAX}: Searches reading buffer for the maximum capacitance value.

$C_A–C_B$: Sequentially computes the difference between corresponding capacitance readings stored in reading buffer A and reading buffer B.

$|V_A–V_B|$: Calculates the corresponding difference in applied voltage for values of capacitance in reading buffer B equal to each value in reading buffer A.

C vs. t: Allows fast measurement of capacitance vs. time (1000 rdg/s).

CABLE COMPENSATION

(Up to 8 setups can be stored in non-volatile memory.)

CALIBRATION CAPACITOR COMPENSATION: Corrects for errors due to cables or switching matrix up to 5 meters effective (electrical equivalent) length. Two measurements are made with cables and matrix terminated with precision reference capacitors in place of the DUT. Model 5907 Cable/Matrix Calibration Capacitor Set required. Bus programmable only. 1MHz only. Accuracy: ±(0.5% + applicable front panel specification), typical.

SINGLE-ENDED CABLE and S-PARAMETER COMPENSATION can also be made. See manual for detailed information.

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590/100k Analog Output Performance

RANGE	ACCURACY (1 Year)[2] 18°–28°C ±(%rdg + counts)	P-P NOISE[3] ANALOG FILTER ON	TEMPERATURE COEFFICIENT 0°–18°C & 28°–50°C ±(%rdg + mV)	SHUNT CAPACITANCE LOADING EFFECT[4] ±(%rdg + mV)
20 pF	1% + $(50 \times G/G_{FS} + 1)$	6 fF	0.2% + $(10 \times G/G_{FS} + 0.1)$	0.1 % + $(0.3 \times G/G_{FS})$
20 µS	1% + $(20 \times C/C_{FS} + 1)$	4 nS	0.2% + $(4 \times C/C_{FS} + 0.1)$	0.1 % + $(0.3 \times C/C_{FS})$
200 pF	1% + $(50 \times G/G_{FS} + 0.5)$	90 fF	0.2% + $(10 \times G/G_{FS} + 0.1)$	0.1 % + $(0.3 \times G/G_{FS})$
200 µS	1% + $(20 \times C/C_{FS} + 0.5)$	60 nS	0.2% + $(4 \times C/C_{FS} + 0.1)$	0.1 % + $(0.7 \times C/C_{FS})$
2 nF	2% + $(50 \times G/G_{FS} + 0.5)$	900 fF	0.4% + $(10 \times G/G_{FS} + 0.2)$	0.02% + $(0.2 \times G/G_{FS})$
2 mS	2% + $(20 \times C/C_{FS} + 0.5)$	0.6 µS	0.4% + $(4 \times C/C_{FS} + 0.2)$	0.02% + $(0.3 \times C/C_{FS})$
20 nF *	3% + $(50 \times G/G_{FS} + 0.5)$[5]	9 pF	0.6% + $(10 \times G/G_{FS} + 0.1)$	0.1 % + $(0.2 \times G/G_{FS})$
20 mS	3% + $(20 \times C/C_{FS} + 0.5)$	6 µS	0.4% + $(4 \times C/C_{FS} + 0.1)$	0.1 % + $(0.2 \times C/C_{FS})$

Accuracy is maximum limit for Q≥20; typical for Q<20.
*Using Model 5904 20nF/20mS Input Adapter.

590/1M Analog Output Performance

RANGE	ACCURACY (1 Year)[2] 18°–28°C ±(%rdg + counts)	P-P NOISE[3] ANALOG FILTER ON	TEMPERATURE COEFFICIENT 0°–18°C & 28°–50°C ±(%rdg + mV)	SHUNT CAPACITANCE LOADING EFFECT[4] ±(%rdg + mV)
20 pF	2% + $(75 \times G/G_{FS} + 1)$	1.2 mV	0.15% + $(15 \times G/G_{FS})$	0.5 % + $(2.5 \times G/G_{FS})$
20 µS	2% + $(30 \times C/C_{FS} + 1)$	0.75 mV	0.15% + $(6 \times C/C_{FS})$	0.5 % + $(1.0 \times C/C_{FS})$
200 pF	3% + $(75 \times G/G_{FS} + 1)$	1.4 mV	0.15% + $(15 \times G/G_{FS})$	0.35% + $(4.0 \times G/G_{FS})$
200 µS	3% + $(30 \times C/C_{FS} + 1)$	0.9 mV	0.15% + $(6 \times C/C_{FS})$	0.35% + $(1.6 \times C/C_{FS})$
2 nF Up to 1nF	5% + $(150 \times G/G_{FS} + 1)$	0.3 mV	0.15% + $(15 \times G/G_{FS})$	0.35% + $(4.0 \times G/G_{FS})$
2 mS Up to 10mS	5% + $(40 \times C/C_{FS} + 1)$	0.2 mV	0.15% + $(6 \times C/C_{FS})$	0.35% + $(1.6 \times C/C_{FS})$
20 nF Above 1nF	5% + $(300 \times G/G_{FS} + 1)$	0.3 mV	0.15% + $(15 \times G/G_{FS})$	0.35% + $(4.0 \times G/G_{FS})$
20 mS Above 10mS	7% + $(40 \times C/C_{FS} + 1)$	0.2 mV	0.15% + $(6 \times C/C_{FS})$	0.35% + $(1.6 \times C/C_{FS})$

NOTES:

1. G = conductance reading; C = capacitance reading; G_{FS} = full scale conductance; C_{FS} = full scale capacitance.
2. Range and accuracy designations based on parallel RC model.
3. Noise specified with 500pF shunt loading on Test Output and Test Input. Noise on 2pF and 20pF ranges is typical with 100pF shunt loading; 500pF will increase noise no more than ×2.
4. "Shunt Capacitance Loading" is additional accuracy with equal shunt load on Test Output and Test Input, per 100pF load.
5. The 5904 must be calibrated with a particular 590/100k to achieve specified accuracy.

TEST VOLTAGE: 15mV rms ±10%.
TEST FREQUENCY: 590/100k: 100kHz. **590/1M:** 1MHz.

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IEEE-488 BUS IMPLEMENTATION

MULTILINE COMMANDS: DCL, LLO, SDC, GET, GTL, UNT, SPE, SPD.

UNILINE COMMANDS: IFC, REN, EOI, SRQ, ATN.

INTERFACE FUNCTIONS: SH1, AH1, TE0, L4, LE0, SR1, RL1, PP0, DC1, DT1, E1, C0 (for stand alone plotting C28 is used).

PROGRAMMABLE PARAMETERS: Range, Function, Zero, Filter, Frequency, Bias Waveform, Bias Parameters, Plotting, Plotter Parameters, EOI, Trigger, Terminator, 450 Data Point Storage, Calibration, Cable Correction, Display, Status, Service Request, Self Test, Output Format.

TRANSLATOR: Up to 250 bytes of definitions allow variable passing, definition decomposition and listing.

ACCESSORIES AVAILABLE

CABLES

7007-1	Shielded IEEE-488 Digital Cable, 1m (3.3 ft)
7007-2	Shielded IEEE-488 Digital Cable, 2m (6.6 ft)
7051-2	BNC Interconnect Cable, 0.6m (2 ft)
7051-5	BNC Interconnect Cable, 1.5m (5 ft)
7051-10	BNC Interconnect Cable, 3m (10 ft)

ADAPTER

5904	20nF/20mS Adapter

CALIBRATION

5905	Calibration Sources for 590/1M
5906	Calibration Sources for 590/100k/1M/4
5907	Cable/Matrix Calibration Sources
5909	Model 82 Calibration Sources

SOFTWARE

Metrics-ICS
Windows-based software for controlling Model 590

Metrics-ICS-CV
Analysis Libraries

TESTPOINT
Graphical programming environment for test

RACK MOUNT KITS

2288	Fixed Rack Mount Kit
2289	Slide Rack Mount Kit

BIAS SOURCE

INTERNAL BIAS SOURCE OUTPUT: –20.000V to +20.000V in 5mV steps.

ACCURACY (1 Year, 18°–28°C): ±(0.05% setting + 10mV) exclusive of loading errors.

DC OUTPUT RESISTANCE: 5Ω maximum.

TEMPERATURE COEFFICIENT (0°–18°C & 28°–50°C): ±(0.005% + 1mV)/°C.

MAXIMUM OUTPUT CURRENT: ±50mA.

SETTLING TIME: <1ms to 1% of final value.

NOISE: Typically <200µV p-p, 0.1Hz-1MHz; 3mV p-p to 75MHz.

BIAS WAVEFORM:

DC: Outputs the programmed value.

STAIR: Output changes in increments of BIAS STEP V from FIRST BIAS V to LAST BIAS V.

DUAL STAIR: Output changes in increments of BIAS STEP V from FIRST BIAS V to LAST BIAS V, then back to FIRST BIAS V.

PULSE: Outputs pulse train; amplitude increments by BIAS STEP V from FIRST BIAS V to LAST BIAS V (each pulse is from DEFAULT BIAS V to FIRST BIAS V for duration of STEP TIME, then back to DEFAULT BIAS V). Also programmable for single pulse.

EXT: Allows application of external bias source (via VOLTAGE BIAS INPUT).

BIAS PARAMETERS: FIRST BIAS V, LAST BIAS V, DEFAULT BIAS V, BIAS STEP V, START TIME, STOP TIME, STEP TIME, COUNT.

BIAS STEP V: Programmable in 5mV steps to 20V. Polarity selectable + or –.

START TIME: After transition from DEFAULT BIAS V to FIRST BIAS V, START TIME must elapse before first measurement. Programmable in increments of 1024µs from 1 to 65,536 increments. **Accuracy:** ±(0.1% + 1ms).

STEP TIME: The period between the transition of BIAS STEP V and the start of the next measurement. Programmable in increments of 1024µs from 1 to 65,536 increments. **Accuracy:** ±(0.1% + 1ms).

STOP TIME: The period between the end of the final measurement and the transition from LAST BIAS V to DEFAULT BIAS V. Programmable in increments of 1024µs from 1 to 65,536 increments. **Accuracy:** ±(0.1% + 1ms).

VOLTAGE BIAS MONITOR: Rear panel output terminals allow monitor of the DC BIAS SOURCE output or externally applied VOLTAGE BIAS INPUT. **Level:** 1V = 1V out. **Output Resistance:** 1kΩ.

EXTERNAL VOLTAGE BIAS INPUT: Rear panel input terminals allow application of external bias source up yo ±200V, ±50mA. **Input Impedance:** 100kΩ paralleled by 1µF.

VOLTAGE BIAS DISPLAY: Front panel 4½-digit display allows direct readback of the DC BIAS SOURCE output or externally applied VOLTAGE BIAS INPUT. **Accuracy:** ±(0.05% + 5 counts). **Temperature Coefficient:** ±(0.005% + 0.1 count)/°C.

GENERAL

DISPLAY: Three 4½-digit displays for capacitance, conductance, and voltage bias.

RANGE: Manual or autoranging (for rates up to 18 rdg/s); 10% overrange allowable.

OVERRANGE INDICATION: Display reads OFLO.

AVAILABLE MEASUREMENT RATES (to internal buffer): 4½-Digit: 1, 10, and 18 rdg/s. **3½-Digit:** 75 and 1000 rdg/s.

FILTER: 1-pole analog; pole at 37Hz. Filters both capacitance and conductance signals. For FILTER off, multiply p-p noise specification by 5.

CAL: Initiates self-calibration to internal reference capacitor. Used to cancel initial zero, gain, and phase errors.

ZERO: Allows zeroing of on range readings. Allows relative readings to be made with respect to a baseline value.

MAXIMUM OVERLOAD:

OUTPUT, Voltage Bias Input: 200V internally fused at 1/8A.

Input: Clamped by diodes to ±0.7V.

Maximum Current: 200mA.

Analog Outputs: 15V.

MAXIMUM COMMON MODE VOLTAGE (INPUT and OUTPUT, Voltage Bias Input): 30V rms, DC to 60Hz. Rear panel switch allows connection of INPUT low to chassis.

ANALOG OUTPUTS (Capacitance and Conductance):
Level: 2V output at full range.
Initial Offset: ±25mV.
Output Resistance: 1kΩ.
Response Time: 1ms to 1% of final value with filter off; 25ms maximum with filter on.

PLOTTER: Digital plotter output controls HP7470A plotter or equivalent using HPGL® via IEEE-488 for real-time plotting of all measurements as well as results of math computations, with grids and labels. Talks to plotter on address 05. HPGL® commands used are IN, IP, IW, PA, PD, PU, SC, SI, SP.

FRONT PANEL SETUPS: Up to 7 front panel setups can be stored in nonvolatile memory.

EXTERNAL TRIGGER: TTL compatible External Trigger Input and Output.

INPUT CONNECTORS: Isolated BNC for INPUT and Voltage Bias Input.

OUTPUT CONNECTORS: Isolated BNCs for OUTPUT, Voltage Bias Monitor, and Analog Outputs. Non-isolated BNCs for External Trigger.

ENVIRONMENT: Operating: 0°–50°C, relative humidity 70% non-condensing up to 35°C. **Storage:** –25° to +65°C.

WARM-UP: 1 hour to rated accuracy.

COOLING: Internal fan and filter for forced air cooling.

POWER: 105–125V or 210–250V (external switch selected), 50Hz to 60Hz, 100VA maximum. 90–110V and 180–220V version available upon request.

DIMENSIONS, WEIGHT: 133mm high × 435mm wide × 448mm deep (5¼ in × 17⅛ in × 17⅝ in). Net weight 9.1kg (20 lb).

ACCESSORIES SUPPLIED: Two Model 7051-5 BNC cables.