

# Attenuation Control Unit Security Features and Volatility Documentation

This manual provides documentation  
for the following instrument:  
J7201A/B/C



Security Features  
and Volatility  
Documentation

## Memory Information and Procedures

Product: J7201A/B/C

Date: 17 October 2019

<b>Memory Type:</b> NAND FLASH Section 1	<b>Memory Size:</b> 2Gbit
<b>Memory Function:</b> Contains the instrument's firmware, failsafe firmware, FPGA image and file system	
<b>User Modifiable (Y/N):</b> N	<b>Volatile (Y/N):</b> N
<b>Memory Erase Processes:</b> <ul style="list-style-type: none"> <li>• Not applicable.</li> <li>• Contains no application specific informations</li> </ul>	

<b>Memory Type:</b> NAND FLASH Section 2	<b>Memory Size:</b> 8Kbit
<b>Memory Function:</b> Contains user configuration data and attenuator cycle count.	
<b>User Modifiable (Y/N):</b> Y	<b>Volatile (Y/N):</b> N
<b>Memory Erase Processes:</b> <ul style="list-style-type: none"> <li>• User can performs factory reset and cycle count clear to restore to factory default setting.</li> <li>• This procedure is not recommended for use in routine applications because of possibility of unintended loss of user data.</li> </ul>	

<b>Memory Type:</b> NAND FLASH Section 3	<b>Memory Size:</b> 5Mbit
<b>Memory Function:</b> Contains corrected data.	
<b>User Modifiable (Y/N):</b> N	<b>Volatile (Y/N):</b> N
<b>Memory Erase Processes:</b> <ul style="list-style-type: none"> <li>• This is only applicable to factory or service only.</li> </ul>	

<b>Memory Type:</b> EEPROM	<b>Memory Size:</b> 32Kbit
<b>Memory Function:</b> Contains basic instrument information such as Board ID, Revision ID, MAC address and Serial number.	
<b>User Modifiable (Y/N):</b> N	<b>Volatile (Y/N):</b> N
<b>Memory Erase Processes:</b> <ul style="list-style-type: none"> <li>• This is only applicable to factory or service only.</li> <li>• No user settable information in this memory.</li> </ul>	

<b>Memory Type:</b> SDRAM DDR	<b>Memory Size:</b> 2Gbit
<b>Memory Function:</b> When the instrument is power on all of the information is downloaded into the SDRAM for use by instrument.	
<b>User Modifiable (Y/N):</b> N	<b>Volatile (Y/N):</b> Y
<b>Memory Erase Processes::</b> <ul style="list-style-type: none"> <li>• Power cycle of the unit earases all volatile memory.</li> </ul>	

<b>Memory Type:</b> NOR FLASH (FPGA)	<b>Memory Size:</b> 32Mbit
<b>Memory Function:</b> Contains main board FPGA binary file.	
<b>User Modifiable (Y/N):</b> N	<b>Volatile (Y/N):</b> N
<b>Memory Erase Processes::</b> <ul style="list-style-type: none"> <li>• Not applicable.</li> <li>• Contains no application specific informations</li> </ul>	

Select one of the following:

- Sanitization process is documented above**
- Sanitization process could be available with engineering resources
- Sanitization process is not possible (i.e. sanitize the product by destruction)



This information is subject to change without notice.

© Keysight Technologies 2019  
Edition 1, October 2019



5992-3901EN

[www.keysight.com](http://www.keysight.com)